

Appl. No. 10/780,075  
Amdt. dated 3/2/06  
Reply to Office action of December 8, 2005

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of Applicants' certified copy of the priority document for German Patent Application 101 20 053.6, filed April 20, 2001 supporting the claim for priority under 35 U.S.C. § 119.

In "Claim Rejections - 35 USC § 112", item 3 on page 2 of the above-identified Office Action, claim 12 has been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that only the conductive layer of the upper electrode is formed of metal. However, the last paragraph on page 29 of the instant application states that the lower capacitor electrode can be metallic or non-metallic.

Therefore, claim 12 has not been changed and it is believed that the claim meets the requirements of 35 U.S.C. § 112, second paragraph.

In "Claim Rejections - 35 USC § 102", item 5 page 3 of the Office Action, claims 8-10 and 14 have been rejected as being

Appl. No. 10/780,075

Amdt. dated 3/2/06

Reply to Office action of December 8, 2005

fully anticipated by U.S. Patent No. 6,552,380 to Sato et al.  
(hereinafter Sato) under 35 U.S.C. § 102(e).

In "Claim Rejections - 35 USC § 103", item 8 on pages 4-5 of the Office Action, claims 12-13 have been rejected as being obvious over Sato in view of U.S. Patent No. 6,335,238 to Hanttangady et al. (hereinafter Hanttangady) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references. However, claim 8 has been slightly amended and new claims 36-41 have been added. Claims 8-10 and 12-14 now relate to the embodiment of the invention wherein the lower capacitor electrode is the conductive layer. New claims 36-41 relate to the embodiment of the invention wherein the upper capacitor electrode is the conductive layer. In this regard, it is noted that claims 37-41 are otherwise identical to claims 9-10 and 12-14, respectively.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 8 now calls for, *inter alia*, a storage capacitor, comprising:

Appl. No. 10/780,075

Amdt. dated 3/2/06

Reply to Office action of December 8, 2005

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

said lower capacitor electrode being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

Independent claim 36 calls for, *inter alia*, a storage capacitor, comprising:

a substrate having a trench formed therein, said trench having a bottom, an upper portion and a lower portion with sidewalls;

a collar disposed in said upper portion of said trench;

a lower capacitor electrode;

a storage dielectric covering said lower portion of said trench and said collar;

an upper capacitor electrode being a conductive layer disposed at said sidewalls of said lower portion of said trench and at said bottom of said trench;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric, said doped layer or said filling covering

Appl. No. 10/780,075  
Amdt. dated 3/2/06  
Reply to Office action of December 8, 2005

said upper capacitor electrode and said storage dielectric at said upper portion of said trench; and

said storage dielectric and said upper capacitor electrode having no doped SiGe layer disposed therebetween.

The Sato reference discloses a semiconductor device including a trench capacitor. A trench having an upper portion and a lower portion is disposed in a substrate. The semiconductor device includes a collar disposed at the upper portion of the trench. A dielectric is disposed on sidewalls at the upper portion of the trench, at the lower portion of the trench, and at a top surface of the substrate. A polysilicon layer is disposed on the dielectric layer and a silicon germanium filling is disposed on the polysilicon layer and fills the trench.

Hanttangady relates to a trench capacitor for use in a DRAM. A trench is disposed in a substrate. The trench capacitor includes an outer electrode formed in the substrate, a silicon carbide layer lining sidewalls of the trench, a high permittivity storage dielectric covering the silicon carbide layer, and an inner electrode of a metal such as titanium nitride or a tungsten-based conductor covering the silicon carbide layer and filling the trench.

The subject matter of independent claim 8, which states that

Appl. No. 10/780,075  
Amdt. dated 3/2/06  
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the lower electrode is the conductive layer, is neither taught nor suggested by the prior art made of record.

The storage capacitor according to independent claim 36 differs from the storage capacitor of Sato by the fact that according to claim 36, the doped layer or filling covers the storage dielectric at the upper portion of the trench, whereas according to Sato the silicon germanium filling covers the polysilicon layer at the upper portion of the trench.

According to Sato, the process of fabricating the semiconductor device includes the deposition of a polycrystalline silicon as a liner film on the entire surface of the trench, the deposition of a silicon germanium film on the polycrystalline film process and flowing the silicon germanium film to fill the trench by performing a heat treatment on the silicon film. According to column 6, line 65 to column 7, line 4, the polysilicon film membrane acts as an appropriate liner film with respect to the silicon germanium film and only the silicon germanium film can be flowed during the heating step. There is no indication, that the silicon germanium film may be flowed according to Sato with a dielectric layer disposed at the upper portion of the trench, as required by claim 36 of the instant application.

Appl. No. 10/780,075  
Amdt. dated 3/2/06  
Reply to Office action of December 8, 2005

Therefore, the storage capacitor according to claim 36 is neither taught nor suggested by Sato.

Clearly, neither Sato nor Hanttangady show or suggest a lower capacitor electrode being a conductive layer as recited in claim 8 of the instant application, and neither Sato nor Hanttangady show or suggest a doped layer or filling covering a storage dielectric at an upper portion of a trench, as recited in claim 36 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 8 and 36. Claims 8 and 36 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 8 or 36.

In view of the foregoing, reconsideration and allowance of claims 8-10, 12-14 and 36-41, are solicited.

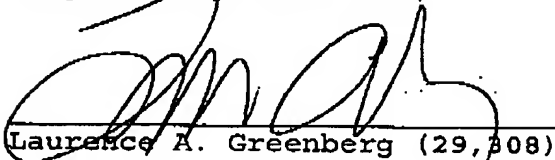
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Appl. No. 10/780,075  
Amdt. dated 3/2/06  
Reply to Office action of December 8, 2005

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner Greenberg, Stemer LLP, No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



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LAG/am

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